



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,905	04/04/2001	Geoffrey S. Strongin	2000.050200 TT3965	3699
23720	7590	05/24/2005	EXAMINER	
WILLIAMS, MORGAN & AMERSON, P.C. 10333 RICHMOND, SUITE 1100 HOUSTON, TX 77042			TSAI, SHENG JEN	
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 05/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/825,905

Applicant(s)

STRONGIN ET AL.

Examiner

Sheng-Jen Tsai

Art Unit

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 April 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 08/01/2003.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 are presented for examination in this application (09,825,905) filed on April 4, 2001.

Acknowledgement is made to the Information Disclosure Statement received on August 1, 2003.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 7-9, 11-13, 15-17, 19-21, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Nozue et al. (US 5,890,189).

As to claim 1, Nozue et al. disclose **a method for providing security in a computer system** [Memory Management and Protection System for Virtual Memory in Computer System (title)], **comprising:**

identifying information for protection [figure 3 shows the protection for both instruction (14) and data (15) memory];

indicating at least one physical address of a memory that houses the information as at least one of read and write disabled [figure 11 shows the protection associated with a plurality of address space, the protection bits including the read permission bit (91), the write permission bit (92), and the execution permission bit (89)] ;

receiving a request from a program to access the information [a program number uniquely assigned to each program is utilized to distinguish a plurality of programs which can make access to the memory (column 1, lines 21-26)] ; and **accessing the information in response to determining that the program has the authority to access the information** [a dedicated memory region can be secured for each program by assigning a unique program number available only to that program (column 1, lines 55-61)].

As to claim 2, Nozue et al. disclose that **indicating at least one physical address of the memory includes: generating a table based on the physical addresses of the memory** [figure 11 shows the table associated with a plurality of physical address space; figure 43; figure 45]; and **indicating in the table that the memory housing the information is at least one of read and write disabled** [figure 11, figure 5D].

As to claim 3, Nozue et al. disclose that **the table is a bitmap based on physical addresses of the memory** [figures 11, 43, and 45].

As to claim 4, Nozue et al. disclose that **the program is an operating system** [the program may be an operating system (column 3, lines 21-26)].

As to claim 7, Nozue et al. disclose **a method for providing security** [Memory Management and Protection System for Virtual Memory in Computer System (title)], **comprising:**

writing to at least one register to define a privileged memory region [a current memory protection information register, figure 3, 17; column 13, lines 35-67];

defining at least one computer instruction as a privileged instruction, wherein the privileged instruction is resident in the privileged memory region [figure 3, 14 shows the instruction access permission signal generator which defines and controls the access to a privileged memory (i.e. the instruction) region. Note that each instruction inside the privileged memory region is treated as a privileged instruction]; **identifying information for protection** [figure 3 shows the protection for both instruction (14) and data (15) memory]; **indicating at least one physical address of a memory that houses the information as at least one of read and write disabled** [figure 11 shows the protection associated with a plurality of address space, the protection bits including the read permission bit (91), the write permission bit (92), and the execution permission bit (89)]; **and controlling the access to the information using the privileged instruction** [a dedicated memory region can be secured for each program by assigning a unique program number available only to that program (column 1, lines 55-61)].

As to claim 8, Nozue et al. disclose **writing to a second register, wherein the first and second registers define the privileged memory region** [figure 3 shows a second register, a target memory protection information register (18, column 13, lines 35-67); figure 43 further shows that two registers (the start and end address registers) that defines the protection region].

As to claim 9, refer to "As to claim 2."

As to claim 11, refer to "As to claim 1." Further, figures 48, 50, and 54 show the program flow diagrams that implement the protection mechanism].

As to claim 12, refer to "As to claim 2."

As to claim 13, Nozue et al. disclose that **the table includes an entry specifying access rights to the information** [figure 43 shows which program ID has the right to access which memory region].

As to claim 15, refer to "As to claim 1."

As to claim 16, refer to "As to claim 2."

As to claim 17, refer to "As to claim 4."

As to claim 19, refer to "As to claim 1." It should be noted that although the figures do not show a processor, it is understood that a computer system inherently has at least one processor.

As to claim 20, refer to "As to claim 2."

As to claim 21, refer to "As to claim 4."

As to claim 24, refer to "As to claim 1."

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5-6, 10, 14, 18, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozue et al. (US 5,890,189), and in view of Childs, Jr. et al. (US 4,442,484).

With respect to claims 5, 10, 14, 18, and 22, Nozue et al. do not mention that **the information is at least one of interrupt descriptor table, global descriptor table, and local descriptor table**. However, Childs, Jr. et al. teach in their invention "Microprocessor Memory Management and Protection mechanism" a memory management and protection mechanism in which access to protected entities is controlled. The protected entities include main memory segments, gates, task state segments, and descriptor tables (column 4, lines 17-24). Particularly, the descriptor tables under protection are three classes of descriptor tables: interrupt descriptor table, global descriptor table, and local descriptor table (column 5, lines 20-40). Providing protection for these descriptor tables allows full multitasking, real-time executive with task, communications, and space management facilities, as more complex microcomputer systems are usually interrupt driven (column 1, lines 20-23). Therefore, it would have been obvious for ones of ordinary skills in the art at the time of Applicants' invention to recognize the benefits of offering protection for descriptor tables, as demonstrated by Childs, Jr. et al., and to incorporate it into the existing memory protection mechanism disclosed by Nozue et al. to further enhance the performance of the system.

As to claim 6, Childs, Jr. et al. teach that **accessing the information in response to determining that the program has the authority to access the**

Art Unit: 2186

information includes using a stack of the computer system to verify the identity of the program [information is pushed on the stack (column 9, lines 30-40).

As to claim 23, Childs, Jr. et al. teach that the processor disclosed in their invention is a microprocessor of the **Intel 8086** family (column 1, lines 9-19).

6. Related Prior Art

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Lai, (US 5,075,842), "Disabling Tag Bit Recognition and Allowing Privileged Operations to Occur in an Object-Oriented Memory Protection mechanism."
- Elward, (US 3,970,999), "Memory Expansion Apparatus"
- Freeman et al., (US 4,677,546), "Guarded Regions for Controlling Memory Access."
- Samson et al., (US 5,995,750), "Memory Protection System for a Multi-Tasking System."
- Devanagundy et al., (US 6,148,384), "Decoupled Serial Memory Access with Passkey Protected Memory Areas."

Conclusion

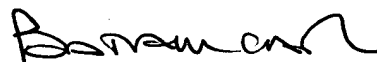
7. Claims 1-24 are rejected as explained above.
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

May 17, 2005


PIERRE BATAILLE
PRIMARY EXAMINER

5/23/05